

Notice of References Cited	Application/Control No. 09/851,181	Applicant(s)/Patent Under Reexamination VAIDA ET AL.	
	Examiner Tri H. Phan	Art Unit 2661	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,363,444 B1	03-2002	Platko et al.	710/110
	B	US-6,260,087 B1	07-2001	Chang, Web	710/100
	C	US-6,263,388 B1	07-2001	Cromer et al.	710/107
	D	US-4,969,121 A	11-1990	Chan et al.	710/113
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Vaidar, Theodore, PLC advanced technology demonstrator TestChipB, LSI Logic Corp, May 2001, IEEE, 0-7803-6591, pages 67-70.
	V	Wilton et al., Programmable Logic IP Cores in SoC Design: Opportunities and Challenges, University of British Columbia, Canada, IEEE, 0-7803-6591, pages 63-66.
	W	Hallschmid et al., Detailed Routing Architectures for Embedded Programmable Logic IP Cores, Department of Electrical and Computer Engineering, University of British Columbia, Canada, February 2001, pages 69-74.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.